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TRANSMITTAL FORM

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Application Number	10/086,980
Filing Date	March 1, 2002
First Named Inventor	Osman Kent
Art Unit	2671
Examiner Name	Tung, Kee M.
Attorney Docket Number	TD-168

Total Number of Pages in This Submission

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
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- ☐ After Allowance Communication to TC
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Remarks

Submission of Reply Brief

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Groover & Holmes Customer No. 29106		
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Date	February 14, 2006	Reg. No.	30,059

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Typed or printed name	Sarah Lau	Date	February 14, 006

In the United States Patent and Trademark Office

In re application of:	:
Kent	:Art Unit: 2676
AN 10/086,980	:Examiner: Tung, Kee M.
Filed: 03/01/2002	:Atty's Docket: TD-168

For: Yield Enhancement of Complex Chips (confirmation no. 6304)

REPLY BRIEF

Honorable Commissioner of Patents and Trademarks
Alexandria, VA 22313

Sir:

Under 37 CFR §41.41(a)(1), Appellant respectfully submits the following Reply Brief in response to Examiner Tung's Answer mailed 1/12/2006.

1) Examiner Tung suggests that it is "well known in the art to dynamically load balanced among multiple processors include skip or bypass defective unit(s)." Examiner Tung has not provided any evidence to support this assertion, and the undersigned attorney is not aware of any GENERAL teaching of this proposition in the prior art. (If there is such a general teaching the Examiner should reopen prosecution and cite it.) Such an asserted teaching is not a proper subject of official notice: either the art teaches this general rule, or it does not.

2) Asserted Combination Inoperative: Examiner Tung suggests that the four "functionally distinct" processing units of Baldwin ('853) Claim 1 are parallelized, presumably because they are pipelined. However, since the units are stated to be functionally distinct, it would seem that bypassing one unit would eliminate its particular function. It also seems that load balancing techniques, as argued by Examiner Tung, could not be applied to a normal pipeline configuration, because ALL tasks pass through each stage of

the pipeline. The Examiner has also not shown how bypassing one unit in a pipeline would be done without breaking the pipeline, and thus disabling the whole unit. Thus the stated combination would seem to be inoperative in THREE ways.

3) APPLICANT ADMITS that parallelized graphics computation units are not novel *per se*. The '853 Baldwin patent itself, at Column 3 lines 26-40, states:

> **Background: Parallelism in Graphics Processing**
>
> **Due to the large number of at least partially independent operations which are performed in rendering, many proposals have been made to use some form of parallel architecture for graphics (and particularly for rendering). See, for example, the special issue of Computer Graphics on parallel rendering (September 1994). Other approaches may be found in earlier patent filings by the assignee of the present application and its predecessors, e.g. 5,195,186, and published PCT applications PCT/GB90/00987, PCT/GB90/01209, PCT/GB90/01210, PCT/GB90/01212, PCT/GB90/01213, PCT/GB90/01214, PCT/GB90/01215, and PCT/GB90/01216.**

Even within a pipelined architecture, an individual graphics processing block may be parallelized: as stated e.g. in the Abstract of Baldwin '853, "**Preferably some of the individual units include parallel paths internally.**"

4) Brent et al. '864 shows real-time recovery from a failed data-movement processor. However, note that Brent's "processors" simply perform data movement operations, and do not appear to perform any computational functions, let alone "graphics computational" functions.

5) Not all integrated circuit programmable devices are analogous, and Brent et al. relates to data transfer operations, which has NOT been shown to be analogous to rendering, nor to any other kind of graphics computation.

6) Regarding motivation: no reason has been shown why one of ordinary skill, looking at Baldwin '853, would seek to improve it with Brent et al. Nothing in the art of record suggests that parallelized graphics

computational units were regarded as fungible elements which could be bypassed; this seems to be a fundamental new teaching of the present application.

7) Note that the Examiner has still not addressed all the specific limitations of the many claims which have been separately argued, including e.g. independent Claims 1, 12, 20, 28, among others.

REQUESTED RELIEF

The Board is respectfully requested to reverse the outstanding rejections.

Respectfully submitted,

2/14/06

Date

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